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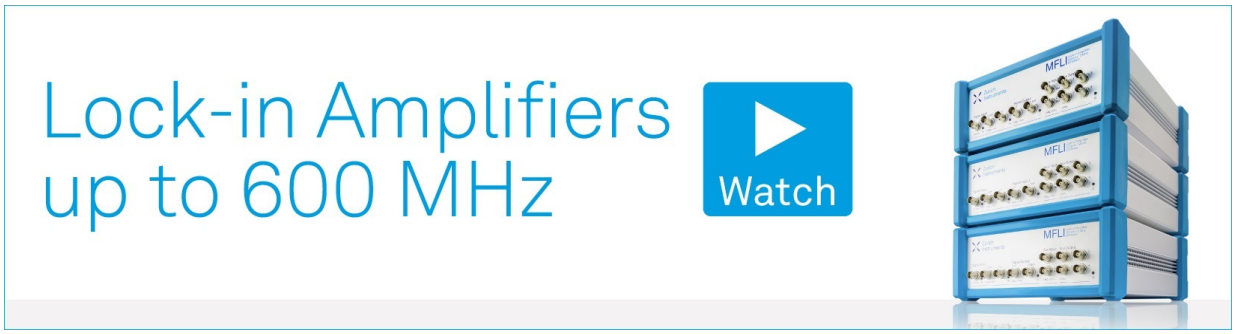

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HTML ABSTRACT + LINKS

Interface states in cycled hot electron injection program/hot hole erase silicon–oxide-nitride–oxide–silicon memories

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Charge pumping measurements were performed to characterize the interface between silicon and bottom oxide in silicon–oxide-nitride–oxide–silicon memory transistors, where information is stored as charges in nitride at the edges of the channel. The charge pumping signal was found to strongly increase with the number of performed program/erase cycles, thus indicating the creation of traps with a density on the order of 10^{12} cm^{-2} (after 100 000 cycles). To estimate the length of the degraded region, the charge pumping signal dependence on the drain voltage was compared with the simulated drain depletion length using TSUPREM/Medici software. The damaged length calculated from the metallurgical junction is about 200 Å at the beginning of the endurance test and increases to 500 Å after 100 000 cycles. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1839289]

This letter deals with the characterization of the dielectric–semiconductor interface in memory field effect transistors with local charge trapping in the oxide–nitride–oxide (ONO) stack by using a charge pumping (CP) technique. Compared with conventional silicon–oxide-nitride–oxide–silicon type flash memory, where charge is stored uniformly in the nitride layer, *micro*Flash® (trademark of Tower Semiconductor Ltd.) memory features localized charge trapping at the edges of the memory transistor channel.[1] Channel hot electron injection is used for programming and band-to-band induced hot hole injection is used for "erasure." A reverse read scheme allows storage of two physical bits per cell, which yields a very dense memory. The thick bottom oxide (BOX) of the ONO does not allow tunneling at low bias, and together with high activation energy of electron and hole traps in the nitride layer ensures excellent retention properties.[2]

A CP method has been applied for the characterization of degradation effects in field effect transistors, nonvolatile memories with polycrystalline silicon floating gates, and nitride memories with the tunnel oxide programmed and erased by Fowler–Nordheim injection from the silicon.[3,4] It was shown that degradation of the ONO–Si interface happens in these devices while the created trap density may exceed 10^{12} cm^{-2}.

In this letter we report on trap generation at the Si–ONO interface in *micro*Flash memory transistors. In these devices the injection of electrons and holes happens through a thick BOX and only in the drain region (the junction with higher bias during programming) of the memory cell. The employed characterization technique is based on CP measurements for programmed and erased devices in combination with numerical simulations using the TSUPREM/Medici software. We show that both the length of the degraded region and the density of the generated interface states are functions of the number of program/erase cycles.

Single cells were fabricated using 0.18 μm Tower Semiconductor Ltd. *micro*Flash technology. The effective channel length, L_{eff}, was 0.22 μm and the transistor (word line) width, W, was 0.18 or 1 μm. Each cell was a part of a field-less cross-wise architecture array with diffusion bit lines and silicided (CoSi) word lines. The effective ONO thickness was 190 Å (70 Å BOX, 60 Å silicon nitride, and 90 Å top oxide). The program window during cycling was 1.6 V. Endurance tests were done to up to 100 000 cycles. The cells were erased to the initial threshold voltage (V_t) to make the degradation effects more pronounced. Programming and erase conditions are specified in Table I.

CP was performed with a constant amplitude of 6 V while the pulse base varied from −8 to 3 V. Trapezoidal pulses with frequencies in the range f=100 kHz–10 MHz were applied to the gate of the memory cell. To ensure proper operation we verified that the CP signal was proportional to the frequency. The source and drain of the memory transistor were connected to a constant bias (0.5–3 V).

Figure 1 shows the CP signal for different numbers of cycles, n, for programmed and erased cells. In both cases, the CP signal increases for larger numbers of cycles indicating the creation of interface states with low time constants ("fast interface states"). The erased state CP peak is shifted to negative values at the V_{base} axis. This is consistent with the mismatch in electron–hole trapping positions in cycled *mi-*

TABLE I. Typical operation conditions of the *micro*Flash memory cells. T_p and T_e represent the program and erase pulse times, respectively.

	V_d (V)	V_g (V)	V_s (V)	T_p/T_e
Program	4.5–5.5	9	0	2 μs
Erase	6–7.5	−4	0.5	2 ms

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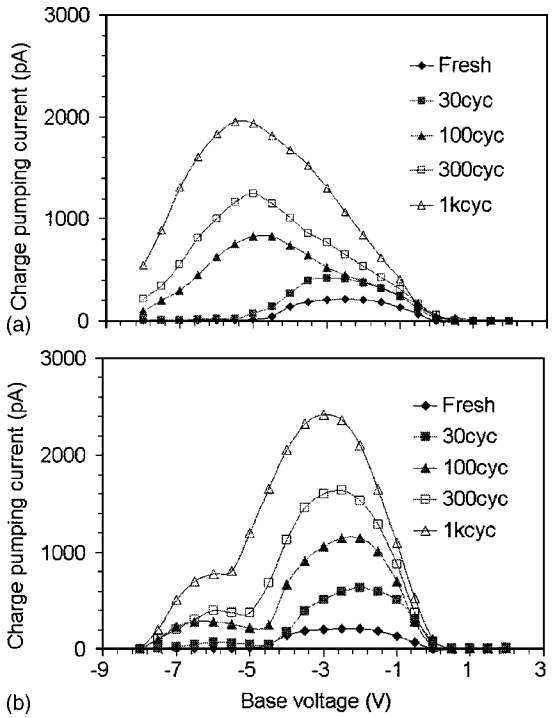

FIG. 1. CP curves for different numbers of cycles. $f=10$ MHz, $L_{\mathrm{eff}}=0.22$ μm, $W=1$ μm.

*cro*Flash memory transistors.[5] The degraded region at the Si–ONO interface in the erased state is located under the positive charge. The value of the positive charge increases with n. The shift of the programmed state CP graph to more positive voltages is weakly pronounced since most of the electrons trapped in the nitride of the programmed cell are above the drain.[6] The second (lower) peak in Fig. 1(b) indicates that positive charge exists in ONO even in the programmed state.

In order to estimate the lateral dimension of the degraded region, the CP signal was measured as a function of the drain bias, V_d. The traps located over the drain and source depletion regions do not contribute the CP current. The dependence of the CP signal of the degraded cell on V_d is presented in Fig. 2. The CP currents decrease with increasing V_d while the peak position shifts to higher V_{base} due to the body bias effect. It is clear that for large enough V_d, the CP signal would reach the level of a fresh cell. The values of the critical drain voltage, V_c, when the CP current disappears

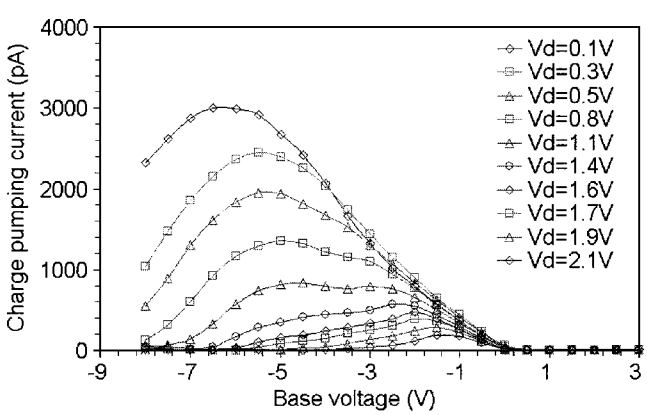

FIG. 2. CP signal for different V_d for cycled erased cell (1000 cycles, $L_{\mathrm{eff}}=0.22$ μm, $W=1$ μm).

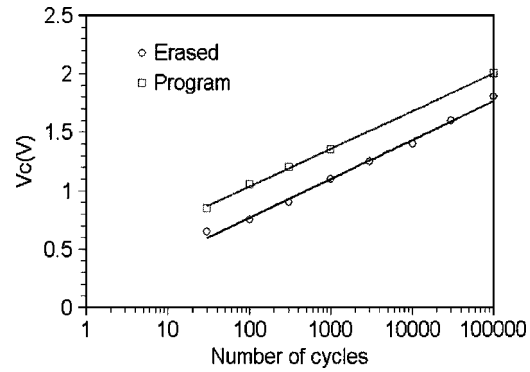

FIG. 3. Critical voltage (V_c) as a function of the number of cycles (n) for programmed and erased cell ($L_{\mathrm{eff}}=0.22$ μm, $W=1$ μm).

are shown in Fig. 3 for both programmed and erased states as a function of n.

The average density of the interface states $N_s(\mathrm{cm}^{-2}\ \mathrm{eV}^{-1})$ that have been generated during cycling can be estimated from the simple expression

$$I_{\mathrm{CP}} = qN_s\Delta EfA, \tag{1}$$

where ΔE is the contributing energy interval in CP measurements (in our case $\Delta E \sim 0.6$–0.7 eV). A is the effective area in the CP experiment, $A=DW$, where W is the device width, $D=X_2-X_1$, X_2 is the length of the region where interface states were generated and X_1 is the drain depletion region at the Si–ONO interface. Both X_1 and X_2 are calculated from the drain metallurgical junction, and were found by two-dimensional numerical simulations using the TSUPREME/Medici software package. The profile of the charge in ONO in the programmed state in V_c simulations was taken from Ref. 6. The length of the degraded region (X_2) and $N_s\ \Delta E$ as functions of n are shown in Fig. 4. The employed bias values in the simulations correspond to the left edge position of the CP curve (Fig. 5). It follows from Fig. 4 that up to $\sim$1000 cycles there is a relatively weak dependence of the interface states density (N_s) on n. However, after 10 000 cycles N_s rapidly increases. The length of the region with the generated interface states after several program/erase cycles is consistent with the injection region length that was estimated in Refs. 6 and 7 and represents the channel part of the memory cell where electrons and holes are trapped. For large numbers of cycles the damaged region significantly widens and reaches $X_2=500$ Å for $n=100\,000$.

Widening of the degraded region (X_2 increase) corresponds to charge trapping far from the drain junction. The electrons that are captured in the created interface states and traps in the BOX are far from the region of hole injection in

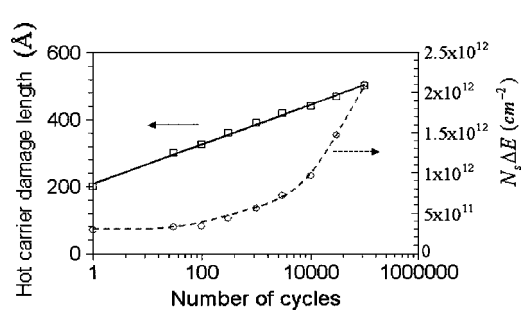

FIG. 4. Length of the degraded region near the drain and N_s in the degraded region as functions of the number of cycles n ($L_{\mathrm{eff}}=0.22$ μm, $W=1$ μm).

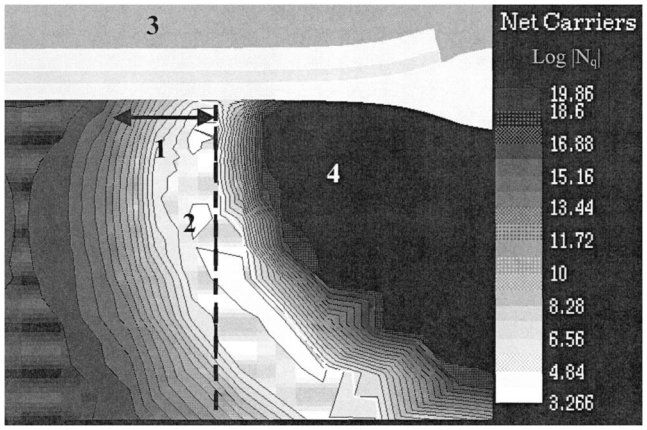

FIG. 5. Concentration of net charge (N_q). The length of the degraded region X_2 is calculated from the metallurgical junction. The gate bias corresponds to the left edge position on the CP curve (accumulation). (1) Degraded region with interface states, $X_2 \sim 500$ A, (2) dashed line shows the position of the metallurgical junction, (3) polycrystalline silicon gate, $V_g = -1$ V, (4) diffusion bit line, $V_d = 1.8$ V.

the erase procedure. In this case more holes are needed for erase. The large amount of holes employed in the erase procedure explains the increase of the trap generation rate for more than 1000 cycles (Fig. 4). The trapped charge can be the cause of the V_t decrease in retention bakes. Electrons trapped in the interface states and in the BOX can be easily detrapped in retention bakes. We argue that after many cycles ($n > 10\,000$) detrapping of electrons captured in the degraded region of the BOX becomes the dominant mechanism for the threshold voltage shift. This is consistent with the observed increasing of the CP current. It was argued[8] that stress induced leakage currents in the bottom oxide are responsible for the charge loss in ONO. In contrast with Ref. 8, the model presented here predicts only a limited charge loss connected with detrapping of electrons from the BOX degraded region aside from the main distribution of electrons in the programmed sate.

In summary, we have studied the generation of surface traps in the drain region of *micro*Flash memory transistors by a charge pumping technique. We demonstrate that the CP current increases with the number of program/erase cycles performed as a result of Si–ONO interface degradation. By performing CP measurements with different voltages at the source and drain in combination with TSUPREME/Medici simulations we were able to find the dependencies of interface state density and the length of the degraded region on the number of cycles, n. The generation rate of interface states strongly increases after 1000 cycles, while the length of degraded region is proportional to log n. The peculiarities of interface state generation in cycling are correlated with the endurance/retention performance of *micro*Flash memory cells.

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